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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,082	07/17/2003	Peter A. Burke	02-0279/1D / LSI1P199D1	3302

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EXAMINER	
BROCK II, PAUL E	

ART UNIT	PAPER NUMBER
2815	

DATE MAILED: 02/15/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/623,082	BURKE ET AL.	
	Examiner	Art Unit	
	Paul E. Brock II	2815	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *19 January 2005*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *19-30* is/are pending in the application.

4a) Of the above claim(s) *20-22* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *19 and 23-30* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Election/Restrictions

1. Claims 20 – 22 are withdrawn from further consideration pursuant to 37 CFR 1.142(b) as being drawn to a nonelected species, there being no allowable generic or linking claim. Election was made **without** traverse in the reply filed on October 6, 2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claim 19 is rejected under 35 U.S.C. 102(b) as being anticipated by Zhao (USPAT 6198170).

With regard to claim 19, Zhao discloses in figures 4 – 6 a method for forming an electrical interconnection structure (430) for connection to large electrical contacts (410). Zhao discloses in figures 4 and 5, and column 14, lines 22 – 28 providing a semiconductor substrate (432/450) having a copper-containing pad layer (422/502) formed thereon such that the copper-containing pad layer includes a plurality of elongate slots (504) having a long axis, a short axis, and sidewalls (adjacent to 504), the slots extending through the pad layer to expose the

underlying semiconductor substrate (underlying substrate in contact with 504). Zhao discloses in figures 4 and 6, and column 15, lines 7 – 24 forming, over the pad layer, a dielectric layer (604) having a plurality of elongate trenches (trenches filled by metal 602) formed therein, the elongate openings having a long axis, a short axis, and sidewalls (adjacent 602) and are configured to extend into the dielectric layer to a depth such that electrical connections to the underlying copper-containing pad layer can be formed. Zhao discloses in figures 4 and 6, and column 15, lines 7 – 24 forming elongate copper-containing contacts (602) in the plurality of elongate openings thereby establishing electrical connections to the underlying copper-containing pad layer. Zhao discloses in figures 4 and 7 – 11 conducting further processing as needed.

Claim Rejections - 35 USC § 103

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. Claim 26 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao in view of Colgan et al. (USPAT 5565707, Colgan).

With regard to claim 26, Zhao discloses in figures 4 – 6 a method for forming an electrical interconnection structure (430) for connection to large electrical contacts (410). Zhao discloses in figures 4 and 5, and column 14, lines 22 – 28 providing a semiconductor substrate (432/450) having a conductive pad layer formed thereon such that the copper-containing pad

layer (422/502) includes a plurality of elongate slots (504) having a long axis, a short axis, and sidewalls (adjacent to 504), the slots extending through the pad layer to expose the underlying semiconductor substrate (underlying substrate in contact with 504). Zhao discloses in figures 4 and 6, and column 15, lines 7 – 24 forming a dielectric layer (604) over the pad layer. Zhao discloses in figures 4 and 6 and column 15, lines 7 – 24 forming a plurality of elongate trenches (trenches filled by metal 602) in the dielectric layer, the elongate trenches having a long axis, a short axis, and sidewalls (adjacent 602) and are configured such that the long axis of the elongate trenches lies transverse to the long axis of the elongate slots in the pad layer to expose a portion of the pad layer wherein the trenches extend sufficiently deep into the dielectric layer so that electrical connections to the underlying conductive pad layer can be formed. It is not clear if Zhao teaches exposing a portion of the sidewalls of the pad layer. Colgan teaches in figure 2 exposing a portion of a sidewall of an underlying feature (30/47) while etching an insulating layer (34). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the exposing a portion of a sidewall of Colgan in the method of Zhao in order to increase the contact area of an overlying feature, and therefore increase current flow through the finished pad structure of Zhao. Zhao discloses in figures 4 and 6, and column 15, lines 7 – 24 filling elongate trenches (602) of the dielectric layer with a conductive material to form conductive contacts which form electrical contacts with the tops of the conductive pad, thereby establishing electrical connection to the underlying conductive pad layer. It would have been further obvious in the method of Zhao and Colgan that electrical contacts are formed with the portions of the sidewalls.

6. Claim 23 is rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao as applied to claim 19 above, and further in view of Colgan et al. (USPAT 5565707, Colgan).

With regard to claim 23, Zhao discloses in figures 4 – 6, and column 15, lines 7 – 24 wherein the step of forming the dielectric layer comprises forming the dielectric layer such that the long axis of the elongate slots lies transverse to the long axis of the elongate trenches in the pad layer to expose a portion of the elongate trenches of the pad layer. It is not clear if Zhao teaches exposing a portion of the sidewalls of the pad layer. Colgan teaches in figure 2 exposing a portion of a sidewall of an underlying feature (30/47) while etching an insulating layer (34). It would have been obvious to one of ordinary skill in the art at the time of the present invention to use the exposing a portion of a sidewall of Colgan in the method of Zhao in order to increase the contact area of an overlying feature, and therefore increase current flow through the finished pad structure of Zhao.

7. Claims 24, 25, and 27 – 30 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zhao and Colgan as applied to claims 19, 23, and 26, respectively, above, and further in view of Simpson (USPAT 6197688).

With regard to claims 24 and 27, Zhao discloses in figures 4 – 6, and column 15, lines 7 – 24 wherein the step of forming elongate copper-containing contacts in the plurality of elongate trenches includes forming a bulk copper containing layer in the elongate slots. It is not clear if Zhao discloses forming at least one barrier layer in the elongate slots and forming a seed layer in the elongate slots. Simpson teaches in figures 7 and 8 forming at least one barrier layer (52) and forming a seed layer (54). It would have been obvious to one of ordinary skill in the art at the

time of the present invention to use the barrier and seed layers of Simpson in the elongate slots in the method of Zhao and Colgan in order to prevent diffusion of copper into the dielectric and other parts of the device, and in order to form the copper layer evenly. Zhao discloses in figures 4 – 6 and column 15, lines 7 – 24 wherein the step of conducting further processing includes removing excess copper-containing materials from a surface of the dielectric layer and electrically connecting the elongate copper-containing contacts to other circuit elements.

With regard to claim 28, Zhao discloses in figure 4 further including the operation of conducting further processing as needed.

With regard to claim 25 and 29, Zhao discloses in figures 4 – 6 wherein the step of conducting further processing includes forming other semiconductor circuit structures (418 – 410).

With regard to claim 30, Zhao discloses in figure 4 wherein the operation of conducting further processing includes forming an electrically conductive top pad (M4) on the dielectric layer wherein the top pad is electrically connected (through V3, M3, V2 and M2) with the conductive contacts.

Response to Arguments

8. Applicant's arguments filed January 19, 2005 have been fully considered but they are not persuasive.

9. With regard to applicant's argument that the "Zhao dielectric D is formed in the openings of the conductive layer only," it should be noted that the rejection does not rely on the dielectric D to teach the claimed dielectric layer. Instead, dielectric 604 is relied upon to teach the claimed subject matter. As shown in figure 6 of Zhao, and in layer 420 of figure 4, dielectric 604 is "over" the metal M1/502 as shown in figure 5 of layer 422 of figure 4. While applicant has pointed to one figure of Zhao, a careful review of all of figures 4 – 6 clearly indicate that 604 is over the conductive layer 502. Therefore, applicant's arguments are not persuasive and the rejection is proper.

10. With regard to applicant's argument that "[figure 2 of Colgan] is not a teaching that the sidewall of the conductive pad should be exposed to enhance the electromigration resistance of a resultant electrical interconnect structure," it should be noted that a reference is good for all that it teaches. In this case, Colgan clearly teaches in figure 2 the claim limitation "to expose a portion of the sidewalls of the elongate trenches of the pad layer." Whether or not this is a desirable feature or an "unintentional artifact" does not preclude Colgan from teaching this claim limitation. Therefore, applicant's arguments are not persuasive and the rejection is proper.

11. With regard to applicant's argument that "Zhao tends to teach away from the idea of exposing the sidewalls to enhance conduction and reduce electromigration," it should be noted that nowhere in Zhao is exposing the sidewalls of the metal M1/522 of layer 422 taught to be an undesirable characteristic. Applicant has failed to point out anywhere in Zhao where exposing the sidewalls would be detrimental to the device or process of Zhao. Applicant's assertion that

the planar surface of layer 422 is not sufficient to teach against the combination. Applicant has not shown how the combination fails. Therefore, applicant's arguments are not persuasive and the rejection is proper.

Conclusion

12. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Paul E. Brock II whose telephone number is (571) 272-1723. The examiner can normally be reached on 8:30 AM - 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on (571) 272-1664. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Paul E Brock II